Enrollment No._____

GANPAT UNIVERSITY

M. Tech. Semester: II Computer Engineering

Regular Examination - MAY 2014

3CE202 : Advanced Computer Architecture

Time: 3 Hours] **[Total Marks: 70**

Instruction: 1 All questions are compulsory.
2 Answer both sections in separate answer sheets.

SECTION - I

Q-1. **(A)** Find out data dependences of the statements of the following program : **7**

```
S1: LOAD  R1, M[100]      /R1 ← M[100]
S2: LOAD  R2, M[104]      /R2 ← M[104]
S3: MULT  R1, R2          /R1 ← R1 * R2
S4: INC R1                /R1 ←R1 + 1
S5: STORE  M[110], R1     /M[110] ←R1
```

Draw a dependency graph to show all the dependences.

(B) Compare Super scalar processor with super pipeline processor using state time diagram and its features. **4**

Q-2. **(A)** An examination paper has 4 questions and total numbers of answer books are 800. each question takes 4 minutes to correct. If 4 teachers are employed for correction and each teacher is responsible to correct 1 question, then define and calculate the speedup and efficiency. **6**

(B) Explain Superscalar Pipeline Structure having 2 pipeline and 4 functional units with diagram. **6**

OR

Q-2. **(A)** Explain different types of data dependence used to determine the ordering relationship between statements with data flow graph. **6**

(B) What are different Vector Instructions used in a typical vector computer? How S-access memory organization is useful in such computers. **6**

Q-3. **(A)** Describe Classification scheme of Pipeline Processors with figure. **6**

(B) "Pipeline processing is more fault tolerant". State True or False & justify your answer with example pipeline diagram. **6**

OR

Q-3. **(A)** Explain FIFO and LRU page replacement scheme in cache memory. And mention benefits of LRU scheme. **6**

(B) Suppose, eight double words can be required for an eight-way interleaved memory system, with 8 logical storage elements, for each memory cycle, having tm = 456 ns. Then find maximum Bandwidth (BWmax), also define and calculate Utilized Memory Bandwidth. **6**

SECTION - II

Q-4. **(A)** Consider the following pipeline reservation table. **7**

	1	2	3	4
S1		X		
S2	X		X	
S3		X		X

(1) Define: Latency Sequence
(2) Find the forbidden set of latencies and collision vector?
(3) Draw the state transition diagram, with required calculation.
(4) List all the greedy cycles.
(5) Determine the minimum average latency.

(B) Main memory is having 4K pages, each page having 16 words while the cache has 128 pages. Then find out no. of bits in a tag field and address of CAM word for (i) 16 pages per set (ii) 32 pages per set **4**

Q-5. **(A)** Explain Synchronization Mechanism in Data Flow Computer Architecture with I-Structure. **6**

(B) How many steps are required to route data from PEi to any other PEj in an Illiac network of N=16 PEs? Justify your answer with diagram showing complete interconnection in network. **6**

OR

Q-5. **(A)** What is the purpose of Overlapping Register Windows in RISC ? Explain Register windows with figure. **6**

(B) In SIMD, explain Generalized Multiprocessor System with diagram containing IPMN, PION, and IPCN networks. **6**

Q-6. **(A)** Define: Dataflow Computer and compare Data flow computer with Control flow computer. **6**

(B) Explain direct mapping technique for mapping of main memory to cache memory. **6**

OR

Q-6. **(A)** List out features of ULTRA SPARC IV plus and also draw its architectural diagram. **6**

(B) What is the basic concept of VLIW? Explain trace scheduling with code compaction using example for VLIW. **6**

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