Exam No: _____

GANPAT UNIVERSITY

M. TECH SEM-II(CE) REGULAR EXAMINATION– APRIL-JUNE 2016

3CE202 : Advanced Computer Architecture

TIME: 3 HRS

TOTAL MARKS: 60

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.

SECTION: I

Q.1(a) Describe both configurations of SIMD Array processor with figure and mention differences between them. (5)

(b) Listout different parallel processing mechanisms and explain balancing of subsystem bandwidth in detail. (5)

OR

Q.1(a) Define: SMT and describe features of Ultra SPARC III processor. (5)

(b) "In cache, the spatial locality among the words in a block decreases with a very large block size." Mention whether statement is True or False & justify your answer with example. (5)

Q.2(a) Explain masking and data routing mechanism of Illiac IV with the help of PE (Processing Elements) and its all registers. (5)

(b) What is the purpose of Overlapping Register Windows in RISC? Explain Register Windows with diagram. (5)

OR

Q.2(a) Why RISC is considered as better performing machine? What are important features of ULTRA SPARC IV plus? Explain with architectural diagram. (6)

(b) In VLIW explain trace scheduling with code compaction using example. (4)

Q.3(a) Explain CAM word and describe block-set associative mapping for cache with diagram. (5)

(b) Explain FIFO and LRU page replacement scheme in cache memory. And mention benefits of LRU scheme. (5)

SECTION: II

Q.4(a) Define pipelining. Why pipelining is needed? Explain it with example. (5)

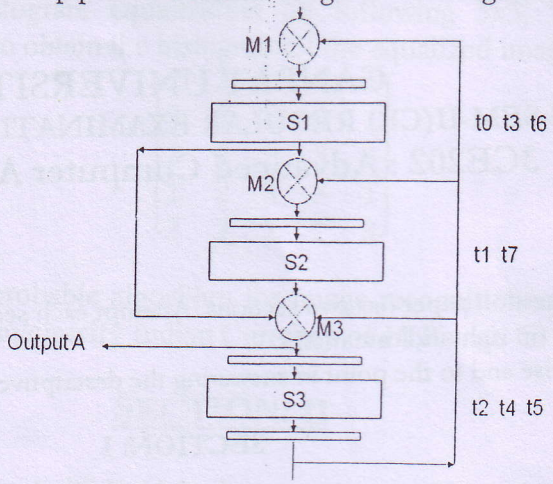
(b) Write the reasons for why maximum speedup limit cannot be achieved in pipeline processor with suitable example. (5)

OR

Q.4(a) Derive the equation for finding the speedup and efficiency of pipelining over non-pipelining processor. (5)

(b) Classify the pipeline processors and explain all in detail with diagram. (5)

Q.5(a) What is linear and non linear pipeline? Consider the given flow diagram:



Answer the following questions:

1. Draw reservation table.
2. Find the evaluation time to get output A.
3. Find feedback and feed forward path.

(b) What is hazard? Define Domain of instruction and Range of Instruction and explain the types of data dependency hazards with example. (5)

OR

Q.5(a) Consider the given reservation table : (6)

	1	2	3	4	5	6
Sa	x					x
Sb		x		x		
Sc			x		x	

Answer the following questions using job sequencing:

1. Find the forbidden set of latencies.
2. State the collision vector.
3. Draw the state transition diagram.
4. List simple cycles and greedy cycles.
5. Calculate MAL (minimum average latency).

(b) Analyze the data dependence among the following statements in a given program fragment and draw a dependence graph to show all the dependences: (4)

S1: LOAD R1, A /R1 ← Memory (A)/
S2: LOAD R2, B / R2 ← Memory (B)/
S3: MUL R1, R2 /R1 ← (R1) * (R2)/
S4: INC R1 /R1 ← (R1) + 1/
S5: STORE B, R1 /Memory B ← (R1)/

Q.6(a) Consider the two instruction I and J. Answer the following questions with reason: (5)

1. If I and J both are Arithmetic & Load type of instruction, then which hazard may be generated?
2. If I is Store type of instructions and J is Arithmetic & Load type of instruction, then which hazard may be generated?
3. If I is Branch type of instructions and J is Arithmetic & Load type of instruction, then which hazard may be generated?

(b) What is Dataflow Computer? How Dataflow Computers are differs with Control Flow Computers? (5)

----------END OF PAPER----------