

**GANPAT UNIVERSITY**  
**M. Tech. SEM-II EC REGULAR EXAMINATION APRIL-JUNE-2016**  
**3EC202 Digital VLSI Design**

MAX TIME: 3 HRS.

MAX MARKS: 60

**Instructions:** (1) This Question paper has two sections. Attempt each section in separate answer book.  
 (2) Figures on right indicate marks.  
 (3) Be precise and to the point in answering the descriptive questions.

### SECTION-I

- 1 (A) Derive expression for depth of depletion region ( $X_d$ ) and amount of charge in depletion region ( $Q$ ) for two terminal MOS. Also find maximum depth of depletion region ( $X_{dm}$ ). (05)
- (B) Draw voltage transfer characteristics (VTC) of resistive load inverter, identify critical voltage points and find expressions of  $V_{OL}$ . (05)

**OR**

- 1 (A) Explain short channel effect and derive the equation for  $\Delta L_D$ . (05)
- (B) Give the comparison of different types of inverter with its VTC. (05)
- 2 (A) Explain the types of MOSFET Capacitances. (05)
- (B) Give the difference between blocking and non-blocking assignment with suitable example. (05)

**OR**

- 2 (A) Explain channel length modulation. (05)
- (B) Derive expression for  $V_{IL}$  for CMOS inverter and explain its operation in detail. (05)
- 3 (A) Design 4 input NAND Gate using pass transistor. (05)
- (B) Write a short note on CMOS ring oscillator. (05)

### SECTION-II

- 4 (A) Explain working principle of CMOS SRAM cell with necessary circuit diagram and waveforms for read and write operation. (05)
- (B) Draw the following CMOS based circuit : (05)
  1. CMOS SR latch based on NOR2
  2. CMOS implementation of the D-Latch

**OR**

- 4 (A) Draw circuit diagram of 3T DRAM cell with its working and related voltage waveforms. (05)
- (B) Implement  $(A+B)C$  using cascade domino CMOS logic (05)
- 5 (A) Draw the circuit diagram of a TSPC based rising edge-triggered DFF (05)
- (B) Explain the concept of charge sharing and explain the method of how to remove it. (05)

**OR**

- 5 (A) Write a spice code for CMOS inverter for DC and transient analysis. (05)
- (B) Draw the PLA implementation of following function : (05)
 
$$F1 = XY + X'Z,$$

$$F2 = Y' + X'Z,$$

$$F3 = XY + Y'Z$$
- 6 (A) Write a short note on latchup. (05)
- (B) Draw the stick diagram layout for half adder. (05)

**End of Paper**