Exam No: _____

GANPAT UNIVERSITY

M. TECH SEM- III ELECTRONICS AND COMMUNITION

REGULAR EXAMINATION NOV-DEC 2016

3EC301 Mixed Signal VLSI Design

MAX. TIME: 3 HRS **MAX. MARKS: 60**

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.

SECTION: I

Q.1(a) Explain following performance specification of DAC. **(05)**
1. Reference Voltages.
2. Settling Time
3. Error

(b) Explain dual-slope ADC. **(05)**

OR

Q.1(a) Explain binary-weighted resistor DAC. **(05)**

(b) Explain flash ADC. **(05)**

Q.2(a) Draw and explain cascode and modified current mirrors. **(05)**

(b) Design a 3-bit DAC using a R-2R architecture with R=1kΩ, R_F=2kΩ and V_{REF}=5V.Assume that the resistance of the switches is negligible. **(05)**

OR

Q.2(a) Explain Basic Current Mirror Circuits with necessary derivations and waveform. **(05)**

(b) Using superposition theorem and half circuit symmetry to derives the AC gain equation of differential amplifier. **(05)**

Q.3(a) What are the advantages of switched capacitor filter circuits compared to RC active filter circuits? **(03)**

(b) Compare analog filter and digital filter circuits. **(03)**

(c) Determine the critical frequency of the Sallen Key low pass filter in Figure 1 and set the value of R1 for an approximate butter-worth response. **(04)**

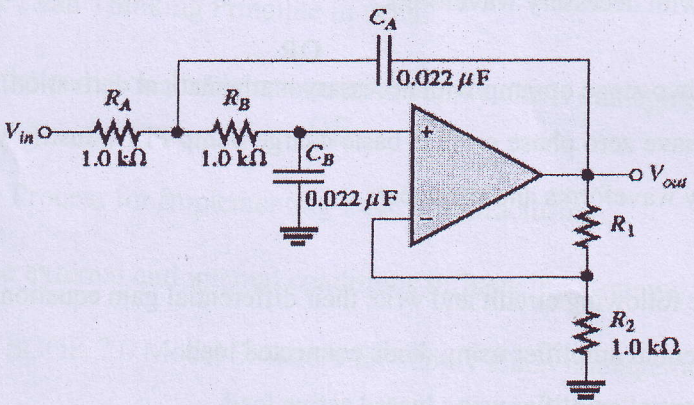

Figure 1

SECTION: II

Q.4(a) Derive transfer function of simple PLL and discuss trade-off between various parameters to improve its performance. **(05)**

(b) Determine the center frequency, maximum gain and bandwidth for the filter in Figure 2. **(05)**

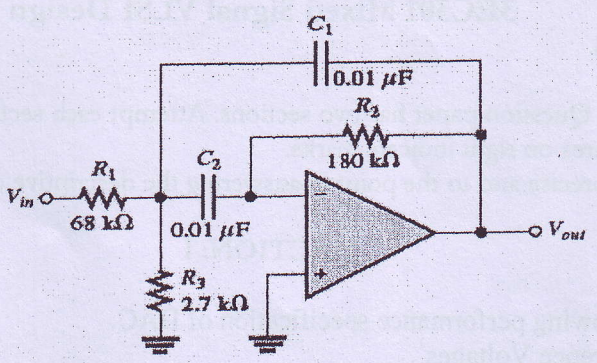

Figure. 2

OR

Q.4(a) Show that the basic charge pump PLL behaves as low-pass filter for the jitter appearing in input signal and it behaves as high-pass filter for the jitter appearing in VCO signal. **(05)**

(b) Draw the circuit diagram of following filter: **(05)**

1. The state variable filter
2. The Biquad Filter

Q.5(a) How can we realize resistor using combination of switches and capacitor? Explain working of basic SC integrator circuit (with two switches), discuss the problems associated with its accuracy and draw SC integrator circuit which solves problem of basic SC integrator circuit. **(05)**

(b) Explain the effect of dead zone in charge pump circuit. How can you avoid it? Explain with necessary waveforms. **(05)**

OR

Q.5(a) Explain two-stage op-amp with necessary mathematical derivation. **(05)**

(b) Can we have zero phase error in basic charge pump PLL? Justify your answer with necessary waveforms and comments. **(05)**

Q.6(a) Draw the following circuit and write their differential gain equation: **(05)**

1. Differential amplifier using diode connected load.
2. Differential amplifier using biased active load.

(b) Explain the following performance parameter for op-amp. **(05)**

(a) Gain (b) Supply and rejection

(c) Linearity

----------**END OF PAPER**----------